WHAT IS CLAIMED IS:

1. A network switch configured to control communication of data frames between stations, comprising:

a plurality of receive devices corresponding to ports on the network switch, the receive devices configured to receive data frames from the stations; and

an external memory interface configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory.

2. The network switch of claim 1, wherein the external memory interface includes:

a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively.

3. The network switch of claim 2, wherein the external memory interface is further configured to simultaneously transfer 8 bytes of data from the first receive device to the first memory and 8 bytes of data from the second receive device to the second memory.

4. The network switch of claim 1, wherein the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second receive devices to the first and second memories.

5. The network switch of claim 1, wherein the external memory interface includes a first external memory bus and a second external memory bus, and the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus.

6. The network switch of claim 5, wherein the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories.

7. The network switch of claim 5, wherein the first and second external memory buses are each 8-bytes wide and operate at a frequency of 100 MHz.

8. The network switch of claim 1, wherein the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus.

9. The network switch of claim 1, wherein the external memory interface is further configured to simultaneously retrieve data from the first and second memories.

10. In a network switch that controls communication of data frames between stations, a method of storing data frame information, comprising:

receiving a plurality of data frames;

temporarily storing the received data frames; and

simultaneously transferring data frame information to at least a first memory and a second memory.

11. The method of claim 10, wherein the data frames are temporarily stored in a plurality of receive devices, further comprising:

simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices.

12. The method of claim 10, wherein the simultaneous data transferring includes:

transferring 8 bytes of data from a first receive device to the first memory and 8 bytes of data from a second receive device to the second memory.

13. The method of claim 10, wherein the simultaneously transferring includes:

sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus.

14. The method of claim 10, wherein the data frames are temporarily stored in a plurality of receive devices, further comprising:

alternately transferring data frame information from a first group of the receive devices to the first and second memories; and

alternately transferring data frame information from a second group of the receive devices to the first and second memories.

15. The method of claim 10, further comprising:

simultaneously retrieving data frame information from the first and second memories.

16. A data communication system for controlling the communication of data frames between stations, comprising:

a plurality of receive devices configured to receive data frames from the stations;

a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices; and

a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus.

17. The system of claim 16, further comprising:

first and second multiplexers coupled to first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame.

18. The system of claim 17, wherein the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external

memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses.

19. The system of claim 16, further comprising:

a first memory coupled to receive data frame information from the first external memory bus and configured to store data words having odd addresses; and

a second memory coupled to receive data frame information from the second external memory bus and configured to store data words having even addresses.

20. The system of claim 19, wherein the switching logic is configured to generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory.